Bachelor and Master Project / Bachelor- und Masterarbeit

Hardware Encryption Engine as a Combination of PRESENT Cipher and RISC-V Processor

Introduction: RISC-V is an open-source instruction set architecture (ISA) using reduced instruction set computer principles. This instruction set is considered an abstract model describing computer components. For instance, certain instructions of RISC-V lead to the implementation and realization of a specific cryptographic engine such as AES or SHA engines. Recently several vendors have started using RISC-V. The number of products using the RISC-V CPU core is expected to be 62.4 billion by 2025.
This project will show the first based on PRESENT cipher. Then, it will show how to develop a new cryptographic RISC-V extensions for efficient implementation of PRESENT cipher. This project aims to develop a secure RISC-V encryption engine by deploying the principles of "Security by Design".

Research Objectives: The work plan contains four steps as follow:

1) Studying and reviewing the recent cryptographic extensions.
2) Studying and investigating PRESENT Cipher.
3) Devising new RISC-V cryptographic extensions for the PRESENT cipher.
4) Implementing the designed RISC-V cryptographic extensions and evaluating the complexity

Applications of the research results:
Jupiter.

Prerequisites/Requirements: Students should have good background in processor design or security , and they should be interested in hardware-implementations.

Starting Date: To be agreed on with the interested party.

Interested students are kindly asked to contact:

- **Instructor and adviser**: Saleh Mulhem, mulhem@iti.uni-luebeck.de
- **Supervisor:** Prof. Dr-Ing, Mladen Berekovic.

Institut für Technische Informatik,
Gebäude 64, 2. Stock,
Universität zu Lübeck
Ratzeburger Allee 160,
23562 Lübeck.